Ref No:

< SRI KRISHNA INSTITUTE OF TECHNOLOGY BANGALORE>

COURSE PLAN

Academic Year 2019-2020

Program:	B E – Information Science & Engineering
Semester :	3
Course Code:	18CS33
Course Title:	Analog and Digital Electronics
Credit / L-T-P:	3 / 3-0-0
Total Contact Hours:	40
Course Plan Author:	Asha B R

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Table of Contents

Note : Remove "Table of Content" before including in CP Book
Each Course Plan shall be printed and made into a book with cover page
Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

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A. COURSE INFORMATION

1. Course Overview

Degree:	BE	Program:	IS
Semester:	3	Academic Year:	2019- 20
Course Title:	Analog and Digital Electronics	Course Code:	18CS33
Credit / L-T-P:	3 / 3-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	40 Hours	SEE Marks:	60 Marks
CIA Marks:	40 Marks	Assignment	1 / Module
Course Plan Author:	Asha B R	Sign ..	Dt:
Checked By:		Sign ..	Dt:
CIA Targets	75%	SEE Target:	68%

Note: Define CIA and SEE % targets based on previous performance.

2. Course Content

Content / Syllabus of the course as prescribed by University or designed by institute. Identify 2 concepts per module as in G.

Module	Module Content	Teaching Hours	Module Concepts	Blooms Level
1	Photodiodes, Light Emitting Diodes and Optocouplers ,BJT Biasing :Fixed bias ,Collector to base Bias , voltage divider bias, Operational Amplifier Application Circuits: Multivibrators using IC-555, Peak Detector, Schmitt trigger, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-to-Voltage and Voltage-to-Current Converter , Regulated Power Supply Parameters, adjustable voltage regulator ,D to A and A to D converter.	8	Diodes Application circuits Opamp application circuits	L3
2	Karnaugh maps: minimum forms of switching functions, two and three variable Karnaugh maps, four variable karnaugh maps, determination of minimum expressions using essential prime implicants, Quine-McClusky Method: determination of prime implicants, The prime implicant chart, petricks method, simplification of incompletely specified functions, simplification using map-entered variables	8	Logic gates fundamentals Boolean equation simplification	L4
3	Combinational circuit design and simulation using gates: Review of Combinational circuit design, design of circuits with limited Gate Fan-in ,Gate delays and Timing diagrams, Hazards in combinational Logic, simulation and testing of logic circuits. Multiplexers, Decoders and Programmable Logic Devices: Multiplexers, three state buffers, decoders and encoders, Programmable Logic devices, Programmable Logic Arrays, Programmable Array Logic.	8	Data processing circuits design Combinational circuit applications	L3
4	Introduction to VHDL: VHDL description of combinational circuits, VHDL Models for multiplexers, VHDL Modules. Latches and Flip-Flops: Set Reset Latch, Gated Latches, Edge-Triggered D Flip Flop 3,SR Flip Flop, J K Flip Flop, T Flip Flop, Flip Flop with additional inputs, Asynchronous Sequential Circuits	8	VHDL models Flip flop Operation	L3
5	Registers and Counters: Registers and Register	8	Register Design	L3

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	Transfers, Parallel Adder with accumulator, shift registers, design of Binary counters, counters for other sequences, counter design using SR and J K Flip Flops, sequential parity checker, state tables and graphs		Counter Design	
-				

3. Course Material

Books & other material as recommended by university (A, B) and additional resources used by course teacher (C).

1. Understanding: Concept simulation / video ; one per concept ; to understand the concepts ; 15 – 30 minutes
2. Design: Simulation and design tools used – software tools used ; Free / open source
3. Research: Recent developments on the concepts – publications in journals; conferences etc.

Module	Details	Chapters in book	Availability
A	**Text books (Title, Authors, Edition, Publisher, Year.)**		-
1 1-5	Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning,2019	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15	In Lib
B	**Reference books (Title, Authors, Edition, Publisher, Year.)**		
1	Anil K Maini, Varsha Agarwal: Electronic Devicesand Circuits, Wiley, 2012.	In Lib	-
2-5	Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 8th Edition, Tata McGraw Hill, 2015	In Lib	In Lib and Dept
2-5	Stephen Brown, Zvonko Vranesic: Fundamentals of Digital Logic Design with VHDL, 2nd Edition, Tata McGraw Hill, 2005.	In Lib	
2-5	R D Sudhaker Samuel: Illustrative Approach to LogicDesign, Sanguine-Pearson, 2010	In Lib	
2-5	M Morris Mano: Digital Logic and Computer Design, 10th Edition, Pearson, 2008.	In Lib	-
C	**Concept Videos or Simulation for Understanding**	-	-
1	https://www.youtube.com/watch?v=jkEVGQ2lneI		
2	https://www.youtube.com/watch?v=-rFOCGT7Xyw		
3	https://www.youtube.com/watch?v=-6w-MHjwzTo		
4	https://www.youtube.com/watch?v=59BbncMjL8I		
5	https://www.youtube.com/watch?v=tsTb-OYsI-M		
6	https://www.youtube.com/watch?v=_yHo2qq82P0		
7	https://www.youtube.com/watch?v=YAlopKvESs0		
8	https://www.youtube.com/watch?v=O5SWZ9i6ySc		
9	https://www.youtube.com/watch?v=-paFaxtTCkI		
10	https://www.youtube.com/watch?v=5vkWccb7uO4		
D	**Software Tools for Design**	-	-
	CircuitMaker, KiCad EDA,ADS Circuit Design Software, Active HDL, Qsapec NGCircuit Design Software,Simulide, OrCAD		
E	**Recent Developments for Research**		
1	http://web.engr.oregonstate.edu/~moon/research/files/Peter_Kiss.pdf		
2	https://www.irjet.net/archives/V3/i5/IRJET-V3I5167.pdf		
3	http://dafx16.vutbr.cz/dafxpapers/14-DAFx-16_paper_59-PN.pdf		
F	**Others (Web, Video, Simulation, Notes etc.)**		
1	https://www.youtube.com/watch?v=qhXZuVFhVzo		
2	https://www.youtube.com/watch?v=YTUHR0Q6Vwo		
3	https://www.youtube.com/watch?v=sUutDs7FFeA		
4	https://www.youtube.com/watch?v=K73N9ES_8nI		
5	https://www.youtube.com/watch?v=XCiLHOZsQI8		

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6	https://www.youtube.com/watch?v=egfHY-NOt6Y		
7	https://www.youtube.com/watch?v=mwJ3uMWvJX0		
8	https://www.youtube.com/watch?v=2ecMG_OciLo		
9	https://www.youtube.com/watch?v=2gqsfgNgN_Y		

4. Course Prerequisites

Refer to GL01. If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.
Students must have learnt the following Courses / Topics with described Content . . .

Modules	Course Code	Course Name	Topic / Description	Sem	Remarks	Blooms Level
	17ELN15 / 17ELN25	Basic Electronics	Knowledge of semiconductors, Knowledge of number systems and boolean algebra	1/2	Gap A seminar on semiconductors, number systems and boolean algebra	L2
-						
-						

5. Content for Placement, Profession, HE and GATE

The content is not included in this course, but required to meet industry & profession requirements and help students for Placement, GATE, Higher Education, Entrepreneurship, etc. Identifying Area / Content requires experts consultation in the area.
Topics included are like, a. Advanced Topics, b. Recent Developments, c. Certificate Courses, d. Course Projects, e. New Software Tools, f. GATE Topics, g. NPTEL Videos, h. Swayam videos etc.

Modules	Topic / Description	Area	Remarks	Blooms Level
	Topics : • Number System and Representation • Programs • Boolean Algebra and Logic Gates • Data Communication	Placement, Profession , GATE and other competitive exams	Recent Developments required to be known for placements and Course projects.	L2
-				
-				

B. OBE PARAMETERS

1. Course Outcomes

Expected learning outcomes of the course, which will be mapped to POs. Identify a max of 2 Concepts per Module. Write 1 CO per Concept.

Modules	Course Code.#	Course Outcome **At the end of the course, student should be able to . . .**	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
1	18CS33.1	Understand the operation of diodes in different application circuits	04	Diodes Application circuits	Lecture	Q & A Unit test	L3
1	18CS33.2	Understand the operation amplifier application circuits	04	Opamp application circuits	Lecture	Q & A Unit test	L3
2	18CS33.3	Understand the fundamentals of logic gates through truth table	04	Logic gates fundamentals	Lecture	Assignment and Slip Test	L4
2	18CS33.4	Simplify Boolean equations by	04	Boolean	Lectur		L4

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		Karnaugh map and Quine MCClusky method to design combinational circuits		equation simplification	e / PPT	Slip test CIA	
3	18CS33.5	Design data processing circuits using combination of gates	04	Data processing circuits design	Lecture	Oral quiz CIA	L3
3	18CS33.6	Understand the fundamentals of combinational circuits by truth table and timing diagram	04	Combinational circuit applications	Lecture	Slip test	L3
4	18CS33.7	Develop and understand the simple VHDL programs for different circuits	04	VHDL models	Lecture	Slip test and assignment	L3
4	18CS33.8	Represent the flip flops as state diagram, characteristic equation	04	Flip flop Operation	Lecture	Assignment and CIA	L3
5	18CS33.9	Illustrate the register and counter properties through truth table and timing diagram	04	Register Design	Lecture / PPT	Quiz CIA	L3
5	18CS33.10	Interpret data conversion techniques through counter using state tables and graphs.	04	Counter Design	Lecture / PPT	Slip test Assignment	L3
-							

2. Course Applications

Write 1 or 2 applications per CO.
Students should be able to employ / apply the course learnings to . . .

Modules	Application Area Compiled from Module Applications.	CO	Level
1	Diodes can be used as rectifiers, signal limiters, voltage regulators, switches, signal modulators, signal mixers, signal demodulators, and oscillators	CO1	L3
1	Opamps are used for current to voltage converter, integrator	CO2	L3
2	Use of logic gates for building combinational circuits	CO3	L4
2	Used to simplification of boolean expressions	CO4	L4
3	Data processing circuits can be used in communication system	CO5	L3
3	Combinational logic is used in computer circuits , such as half adders, full adders, half subtractors, full subtractors, multiplexers, demultiplexers, encoders and decoders.	CO6	L3
4	VHDL hardware description language and its application to digital hardware design and verification.	CO7	L3
4	Flip flops can be used to store the data and frequency divider	CO8	L3
5	Registers are used to store the instructions	CO9	L3
5	Counters are used for counting electronic pulses and also used to convert signals	CO10	L3

3. Mapping And Justification

CO – PO Mapping with mapping Level along with justification for each CO-PO pair.
To attain competency required (as defined in POs) in a specified area and the knowledge & ability required to accomplish it.

Modules	Mapping		Mapping Level	Justification for each CO-PO pair	Level
-	**CO**	**PO**	-	**'Area': 'Competency' and 'Knowledge' for specified 'Accomplishment'**	-
1	CO1	PO1	L3	Knowledge of diodes is required in switching circuits which are used in complex circuits like transmitters and receivers	L3
1	CO1	PO2	L3	Analysing problem in amplifier circuits require knowledge of opamp	L3
1	CO1	PO3	L3	opamp are used in testing devices like oscilloscopes , voltmeters	L3
1	CO1	PO4	L3	No investigations and interpretation content no mapping	L3
1	CO1	PO5	L3	No content tool, no mapping	L3
1	CO1	PO6	L3	No engineering practice	L3

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1	CO1	PO7	L3	No matching for environment and sustainability	L3
1	CO1	PO8	L3	No matching for ethical principles	L3
1	CO1	PO9	L3	3	L3
1	CO1	PO10	L3	No communication	L3
1	CO1	PO11	L3	For project development in area of embedded devices, electronic projects knowledge of FET is useful	L3
1	CO1	PO12	L3	Learning in the context of technology changes .	L3
2	CO2	PO1	L4	Opamps are used in baseband receivers ,signal generators etc	L4
2	CO2	PO2	L4	Knowledge is useful in analysis of communication circuits	L4
2	CO2	PO3	L4	Opamps are used in circuits to perform mathematical operations	L4
2	CO2	PO4	L4	No investigations and interpretation content no mapping	L4
2	CO2	PO5	L4	No content tool, no mapping	L4
2	CO2	PO6	L4	No engineering practice	L4
2	CO2	PO7	L4	No matching for environment and sustainability	L4
2	CO2	PO8	L4	No matching for ethical principles	L4
2	CO2	PO9	L4	For managing the analog circuits in communication individual should require the knowledge of opamps	L4
2	CO2	PO10	L4	No communication	L4
2	CO2	PO11	L4	For project development in area of embedded devices, electronic projects knowledge of opamp is useful	L4
2	CO2	PO12	L4	Learning in the context of technology changes .practice	L4
3	CO3	PO1	L3	logic gates are used in all electronic devices like computers, lifts etc	L3
3	CO3	PO2	L3	knowledge of logic gates is required for analyzing problems in digital circuits	L3
3	CO3	PO3	L3	For designing digital circuits knowledge of logic gates is required	L3
3	CO3	PO4	L3	No investigations and interpretation content no mapping	L3
3	CO3	PO5	L3	No content tool, no mapping	L3
3	CO3	PO6	L3	No engineering practice	L3
3	CO3	PO7	L3	No matching for environment and sustainability	L3
3	CO3	PO8	L3	No matching for ethical principles	L3
3	CO3	PO9	L3	For managing the digital circuits individual should require the knowledge of logic gates	L3
3	CO3	PO10	L3	No communication	L3
3	CO3	PO11	L3	For electronic digital projects knowledge of logic gates is required	L3
3	CO3	PO12	L3	Learning in the context of technology changes .	L3
4	CO4	PO1	L3	Knowledge of K maps helps the students in circuit designing	L3
4	CO4	PO2	L3	Analysis of circuits makes the students better understanding of digital circuits	L3
4	CO4	PO3	L3	Helps the students in design of simple circuits using gates	L3
4	CO4	PO4	L3	No investigations and interpretation content no mapping	L3
4	CO4	PO5	L3	No content tool, no mapping	L3
4	CO4	PO6	L3	No engineering practice	L3
4	CO4	PO7	L3	No matching for environment and sustainability	L3
4	CO4	PO8	L3	No matching for ethical principles	L3
4	CO4	PO9	L3	For developing the digital circuits with minimum gates simplification methods are useful for individual	L3
4	CO4	PO10	L3	No communication	L3
4	CO4	PO11	L3	For digital project development simplification methods are useful	L3
4	CO4	PO1	L3	Learning in the context of technology changes .	L3

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		2			
5	CO5	PO1	L3	Data processing circuits like mux ,demux are used in communication systems	L3
5	CO5	PO2	L3	To analyze the problem in communication systems knowledge of data processing circuits is required	L3
5	CO5	PO3	L3	Encoders and decoders are used in data communication	L3
5	CO5	PO4	L3	No investigations and interpretation content no mapping	L3
5	CO5	PO5	L3	No content tool, no mapping	L3
5	CO5	PO6	L3	No engineering practice	L3
5	CO5	PO7	L3	No matching for environment and sustainability	L3
5	CO5	PO8	L3	No matching for ethical principles	L3
5	CO5	PO9	L3	To manage the digital communication circuits knowledge of data processing circuits is useful	L3
5	CO5	PO10	L3	No communication	L3
5	CO5	PO11	L3	For digital project development knowledge of data processing circuits is useful	L3
5	CO5	PO12	L3	Learning in the context of technology changes .	L3
6	CO6	PO1	L3	Flip flops are basic components of registers which are used in building memory devices	L3
6	CO6	PO2	L3	To analyze the memory of sequential circuits knowledge of flip flops is required	L3
6	CO6	PO3	L3	Design of sequential circuits needs the knowledge of flip flops	L3
6	CO6	PO4	L3	No investigations and interpretation content no mapping	L3
6	CO6	PO5	L3	No content tool, no mapping	L3
6	CO6	PO6	L3	No engineering practice	L3
6	CO6	PO7	L3	No matching for environment and sustainability	L3
6	CO6	PO8	L3	No matching for ethical principles	L3
6	CO6	PO9	L3	To manage the memory in sequential circuits individual require the knowledge of flipflops	L3
6	CO6	PO10	L3	No communication	L3
6	CO6	PO11	L3	For digital electronic projects having memory knowledge of flip flop is required	L3
6	CO6	PO12	L3	Learning in the context of technology changes .	L3
7	CO7	PO1	L3	Flip flop representation is required in design of counters	L3
7	CO7	PO2	L3	No analysis. No mapping	L3
7	CO7	PO3	L3	For digital clock design flip flop representation is required	L3
7	CO7	PO4	L3	No investigations and interpretation content no mapping	L3
7	CO7	PO5	L3	No content tool, no mapping	L3
7	CO7	PO6	L3	No engineering practice	L3
7	CO7	PO7	L3	No matching for environment and sustainability	L3
7	CO7	PO8	L3	No matching for ethical principles	L3
7	CO7	PO9	L3	No team work	L3
7	CO7	PO10	L3	No communication	L3
7	CO7	PO11	L3	No project development	L3
7	CO7	PO12	L3	No lifelong learning .	L3
8	CO8	PO1	L3	Register and counters are sequential logic circuits which are used to construct Finite state machines, a basic building block in all digital circuitry.	L3
8	CO8	PO2	L3	No analysis	L3
8	CO8	PO3	L3	Registers are used in design of memory devices	L3
8	CO8	PO4	L3	No investigations and interpretation content no mapping	L3

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8	CO8	PO5	L3	No content tool, no mapping	L3
8	CO8	PO6	L3	No engineering practice	L3
8	CO8	PO7	L3	No matching for environment and sustainability	L3
8	CO8	PO8	L3	No matching for ethical principles	L3
8	CO8	PO9	L3	For storing and managing the data in memory individual should require the knowledge of registers	L3
8	CO8	PO10	L3	No communication	L3
8	CO8	PO11	L3	Every applications requires memory to store the data and knowledge of registers is required	L3
8	CO8	PO12	L3	lifelong learning & understanding the sequential circuits is essential for digital design	L3
9	CO9	PO1	L3	Counters are basic components of digital clock	L3
9	CO9	PO2	L3	No analysis	L3
9	CO9	PO3	L3	For most of digital applications clock is used	L3
9	CO9	PO4	L3	No investigations and interpretation content no mapping	L3
9	CO9	PO5	L3	No content tool, no mapping	L3
9	CO9	PO6	L3	No engineering practice	L3
9	CO9	PO7	L3	No matching for environment and sustainability	L3
9	CO9	PO8	L3	No matching for ethical principles	L3
9	CO9	PO9	L3	For designing of digital clock individual require th knowledge o design of counters	L3
9	CO9	PO10	L3	No communication	L3
9	CO9	PO11	L3	For electronic projects counter design is useful for dsigning the digital clock	L3
9	CO9	PO12	L3	Learning in the context of technology changes	L3
10	CO10	PO1	L3	Knowledge of ADC and DAC are required building in Broadband communications systems ,Satellite Communications , Radars and jammers	L3
10	CO10	PO2	L3	No analysis	L3

4. Articulation Matrix

CO – PO Mapping with mapping level for each CO-PO pair, with course average attainment.

-	-	Course Outcomes	Program Outcomes														-
Modules	CO.#	**At the end of the course student should be able to . . .**	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	Level
1	18CS33.1	Understand the operation of diodes in different application circuits	3	2	2						2		2	2				L3
1	18CS33.2	Understand the operation amplifier application circuits	3	2	2						2		2	2				L3
2	18CS33.3	Understand the fundamentals of logic gates through truth table	3	2	2						2		2	2				L4
2	18CS33.4	Simplify Boolean equations by Karnaugh map and Quine MCClusky method to design combinational circuits	3	2	2						2		2	2				L4
3	18CS33.5	Design data processing circuits using combination of gates	3	2	2						2		2	2				L3
3	18CS33.6	Understand the fundamentals of combinational circuits by truth table and timing diagram	3	2	2						2		2	2				L3
4	18CS33.7	Develop and understand the simple VHDL programs for different circuits	2		2													L3

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4	18CS33.8	Represent the flip flops as state diagram, characteristic equation	3		2						2		2	2				L3
5	18CS33.9	Illustrate the register and counter properties through truth table and timing diagram	3		2						2		2	2				L3
5	18CS33.10	Interpret data conversion techniques through counter using state tables and graphs.	2		2						2		2	2				L3
-	**CS501PC**	**Average attainment (1, 2, or 3)**																**-**
-	*PO, PSO*	*1.Engineering Knowledge; 2.Problem Analysis; 3.Design / Development of Solutions; 4.Conduct Investigations of Complex Problems; 5.Modern Tool Usage; 6.The Engineer and Society; 7.Environment and Sustainability; 8.Ethics; 9.Individual and Teamwork; 10.Communication; 11.Project Management and Finance; 12.Life-long Learning; S1.Software Engineering; S2.Data Base Management; S3.Web Design*																

5. Curricular Gap and Content

Topics & contents not covered (from A.4), but essential for the course to address POs and PSOs.

Modules	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					

6. Content Beyond Syllabus

Topics & contents required (from A.5) not addressed, but help students for Placement, GATE, Higher Education, Entrepreneurship, etc.

Modules	Gap Topic	Area	Actions Planned	Schedule Planned	Resources Person	PO Mapping

C. COURSE ASSESSMENT

1. Course Coverage

Assessment of learning outcomes for Internal and end semester evaluation. Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

Modules	Title	Teach. Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	Diodes and operation amplifiers	08	2	-	-	1	1	2	CO1, CO2	L3
2	Kmaps and other techniques	08	2	-	-	1	1	2	CO3, CO4	L4
3	Combinational logic circuits	08	-	2	-	1	1	2	CO5, CO6	L3
4	VHDL models and flip flops	08	-	2	-	1	1	2	CO7, C08	L3
5	Register and counters	08	-	-	4	1	1	2	CO9, CO10	L3
-	**Total**	**40**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

2. Continuous Internal Assessment (CIA)

Assessment of learning outcomes for Internal exams. Blooms Level in last column shall match with A.2.

Modules	Evaluation	Weightage in Marks	CO	Levels
1, 2	CIA Exam – 1	30	CO1, CO2, CO3,CO4	L3,L4
3, 4	CIA Exam – 2	30	CO5, C06,CO7,CO8	L3,L3
5	CIA Exam – 3	30	CO9,CO10	L3
1, 2	Assignment - 1	10	CO1, CO2, CO3,CO4	L3,L4
3, 4	Assignment - 2	10	CO5, C06,CO7,CO8	L3,L3
5	Assignment - 3	10	CO9,CO10	L3

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1, 2	Seminar - 1		-	-
3, 4	Seminar - 2		-	-
5	Seminar - 3		-	-
1, 2	Quiz - 1		-	-
3, 4	Quiz - 2		-	-
5	Quiz - 3		-	-
1 - 5	Other Activities – Mini Project	-	-	-
	Final CIA Marks	**40**	**-**	**-**

D1. TEACHING PLAN - 1

Module - 1

Title:	Diodes and Operational amplifier	Appr Time:	08 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
1	Understand the operation of diodes in different application circuits	CO1	L3
2	Understand the operation amplifier application circuits	CO2	L3
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
1	Introduction to Photodiodes	CO1	L2
2	Light Emitting Diodes and Optocouplers	CO1	L3
3	BJT Biasing :Fixed bias ,Collector to base Bias	CO1	L2
4	voltage divider bias, Operational Amplifier Application Circuits	CO1	L3
5	Multivibrators using IC-555, Peak Detector,Schmitt trigger, Active Filters	CO2	L2
6	Non-Linear Amplifier,Relaxation Oscillator, Current-to-Voltage and Voltage-to-Current Converter	CO2	L2
7	Regulated Power Supply Parameters, adjustable voltage regulator	CO2	L3
8	D to A and A to D converter.	CO2	L2
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Diodes can be used as rectifiers, signal limiters, voltage regulators, switches, signal modulators, signal mixers, signal demodulators, and oscillators	CO1	L3
2	Opamps are used for current to voltage converter, integrator	CO2	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	Explain working of photo diode?	CO1	L2
2	List the applications of photo diode.	CO1	L2
3	Explain working of LED?	CO1	L2
4	List the applications of LED.	CO1	L2
5	Explain working of optocoupler?	CO1	L2
6	List the applications of optocoupler.	CO1	L2

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4	What is differences b/w ideal and practical op-amp amplifier?	CO2	L3
8	Explain astable multivibrator using 555 timer?	CO2	L3
9	Explain mono multivibrator using 555 timer?	CO2	L3
10	Explain Comparator? How do you convert sine wave to rectangular output, using Op-Amp?	CO2	L2
9	Explain the ADC circuit?	CO2	L2
10	Explain the DAC circuit?	CO2	L2
11	Explain the working of relaxation oscillator?	CO2	L3
12	Explain the working of SAR?	CO2	L2
13	Write the SAR code conversion tree for 1000.	CO2	L3
e	**Experiences**	-	-
1			
2			

Module – 2

Title:	K maps and other techniques	Appr Time:	08 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
1	Understand the fundamentals of logic gates through truth table	CO3	L4
2	Simplify Boolean equations by Karnaugh map and Quine MCClusky method to design combinational circuits	CO4	L4
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
1	Karnaugh maps: minimum forms of switching functions	CO3	L4
2	Two and three variable Karnaugh maps	CO3	L4
3	Four variable karnaugh maps	CO3	L4
4	Determination of minimum expressions using essential prime implicants	CO3	L4
5	Quine-McClusky Method, determination of prime implicants	CO4	L4
6	The prime implicant chart, Petricks method	CO4	L4
7	Simplification of incompletely specified functions	CO4	L4
8	Simplification using map-entered variables	CO4	L4
c	**Application Areas**	-	-
1	Use of logic gates for building combinational circuits	CO3	L4
2	Used to simplification of boolean expressions	CO4	L4
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	Explain the logic circuit and truth table of the Inverter, OR and AND gate	CO3	L3
2	Why NAND & NOR gates are called universal gates.	CO3	L3
3	Differentiate between positive and negative logic.	CO3	L3
4	Implement AB+CD with only three NAND gates. Draw logic diagram also. Assume the inverted input is available.	CO3	L4
5	Minimize the following using K-maps: if(A,B,C,D)=Σm(0,1,2,3,5,9,14,15)+$\Sigma\Phi$(4,8,11,12)	CO4	L4
6	Derive minimal SOP expression using K map and draw circuit diagram f(a,b,c,d) = $\sum$m(1,4,6,8,9,10,11,12,13)+d(3,15)	CO4	L4
7	Derive minimal POS expression using K map and draw circuit diagram f(a,b,c,d) = πM(1,2,8,9,12,13,14)+d(0,14,15)	CO4	L4
8	What is static-1 hazard? Explain with an example how it can be covered.	CO4	L3
9	Simplify the given expression using Quine Mcclusky method f(a,b,c,d)= $\sum$m(1,2,8,9,12,13,14)	CO4	L4

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E1. CIA EXAM – 1

a. Model Question Paper - 1

Crs Code:	18CS33	Sem:	III	Marks:	50	Time:	90 minutes
Course:	Analog and Digital electronics						

-	-	**Note: Answer all questions, each carry equal marks. Module : 1, 2**	**Marks**	**CO**	**Level**
1	a	What is a photo diode? Explain in detail with construction , working and its applications.	12	CO1	L2
	b	Write a short note on Peak Detector.	8	CO2	L2
	c	Calculate the Max and Min levels of I_C and V_{CE} for the base bias, when β_{min}=50 and β_{max}=200. (Rc = 2.2kΩ , Rb = 470kΩ, Vcc = +18v)	5	CO1	L3
		OR			
2	a	Explain the working of Monostable multivibrator along with wave forms.	12	CO2	L2
	b	Explain Collector to base biasing in detail.	8	CO1	L3
	c	List out the applications of Photo coupler.	5	CO1	L2
3	a	Explain about positive and negative logic, Prove that positive 'OR' is equal to negative AND.	4	CO3	L2
	b	Minimize the following Boolean function using K-map method. f(a,b,c,d) = ∑m (5,6,7,12,13) + ∑d (4,9,14,15).	6	CO3	L4
	c	Simplify the following Boolean function by using Quine-McClusky method to find the essential prime implicants . F(A,B,C,D) = ∑m (0,2,3,6,7,8,10,12,13).	10	CO4	L4
	d	Use MEV method to simplify the following expression. f(a,b,c,d) = ∑m (3,4,5,7,8,11,12,13,15)	5	CO4	L4
		OR			
4	a	Find the minimal SOP for the following Boolean function using K-map. I) f(a,b,c,d) = ∑m (6,7,9,10,13) + ∑d (1,4,5,11,15). ii) f(a,b,c,d) = ∏M (1,2,3,4,10) + ∑d (0,15).	8	CO3	L4
	b	Using Petrick method find the Essential prime implicants for the following Boolean equation. f (a,b,c,d) = ∑m (0,1,2,5,10,11,14,15).	8	CO4	L4
	c	Simplify the function using MEV method taking the variable in the least significant position as the map entered variable. f(a,b,c,d) = ∑m (2,3,4,5,13,15) + ∑d (8,9,10,11).	5	CO4	L4
	d	What are Hazards? Explain the types of hazards.	4	CO4	L2

b. Assignment -1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	18CS33	Sem:	III	Marks:	10	Time:	90 – 120 minutes
Course:	Analog and Digital electronics				Module : 1, 2		
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	USN	Assignment Description	Marks	CO	Level
1		Explain working of photo diode?	10	CO1	L2
2		List the applications of photo diode.	10	CO1	L2
3		Explain working of LED?	10	CO1	L2
4		List the applications of LED.	10	CO1	L2
5		Explain working of optocoupler?	10	CO1	L2
6		List the applications of optocoupler.	10	CO1	L2
7		What is differences b/w ideal and practical op-amp amplifier?	10	CO2	L3
8		Explain astable multivibrator using 555 timer?	10	CO2	L3
9		Explain mono multivibrator using 555 timer?	10	CO2	L3
10		Explain Comparator? How do you convert sine wave to rectangular output, using Op-Amp?	10	CO2	L2
11		Explain the ADC circuit?	10	CO2	L2
12		Explain the DAC circuit?	10	CO2	L2

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13		Explain the working of relaxation oscillator?	10	CO2	L3
14		Explain the working of SAR?	10	CO2	L2
15		Write the SAR code conversion tree for 1000.	10	CO2	L3
		Explain the logic circuit and truth table of the Inverter, OR and AND gate	10	CO3	L3
17		Why NAND & NOR gates are called universal gates.	10	CO3	L3
18		Differentiate between positive and negative logic.	10	CO3	L3
19		Implement AB+CD with only three NAND gates. Draw logic diagram also. Assume the inverted input is available.	10	CO3	L4
20		Minimize the following using K-maps: if(A,B,C,D)=Σm(0,1,2,3,5,9,14,15)+ΣΦ(4,8,11,12)	10	CO4	L4
21		Derive minimal SOP expression using K map and draw circuit diagram f(a,b,c,d) = ∑m(1,4,6,8,9,10,11,12,13)+d(3,15)	10	CO4	L4
22		Derive minimal POS expression using K map and draw circuit diagram f(a,b,c,d) = πM(1,2,8,9,12,13,14)+d(0,14,15)	10	CO4	L4
23		What is static-1 hazard? Explain with an example how it can be covered.	10	CO4	L3
24		Simplify the given expression using Quine Mcclusky method f(a,b,c,d)= ∑m(1,2,8,9,12,13,14)	10	CO4	L4

D2. TEACHING PLAN - 2

Module – 3

Title:	Combinational circuits and applications	Appr Time:	08 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
1	Design data processing circuits using combination of gates	CO5	L3
2	Understand the fundamentals of combinational circuits by truth table and timing diagram	CO6	L3
b	***Course Schedule***		
Class No	**Portion covered per hour**	**-**	**-**
1	Combinational circuit design and simulation using gates	CO5	L2
2	Review of Combinational circuit design	CO5	L2
3	Design of circuits with limited Gate Fan-in	CO5	L3
4	Gate delays and Timing diagrams, Hazards in combinational Logic	CO6	L3
5	Simulation and testing of logic circuits, Multiplexers	CO6	L3
6	Three state buffers, Decoders and encoders	CO6	L3
7	Programmable Logic devices, Programmable Logic Arrays	CO6	L3
8	Programmable Array Logic.	CO6	L3
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Data processing circuits can be used in communication system	CO5	L2
2	Combinational logic is used in computer circuits , such as half adders, full adders, half subtractors, full subtractors, multiplexers, demultiplexers, encoders and decoders.	CO6	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	Explain the gate delays and timing diagrams?	CO5	L2
2	Explain simulation and testing with examples.	CO5	L2
3	Why is a Multiplexer called a Universal logic	CO6	L3

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4	Configure 16 to 1 MUX using 4 to 1 MUX	CO6	L3
5	Implement the f(x,y,z)= ∑m(0,4,5,6) function using 8to1 MUX	CO6	L3
6	Define parity generator and parity checker	CO6	L3
7	Design 3 - 8 decoder	CO6	L3
8	Design a 32 to 1 multiplexer using two 16 to 1 multiplexers and one 2 to 1 multiplexer.	CO6	L3
9	Give seven segment decoder using PLA.	CO6	L3
10	Explain PLA and PAL.	CO6	L2
e	**Experiences**	-	-
1			
2			

Module – 4

Title:	VHDL models and Flip Flops	Appr Time:	08 Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to . . .	-	**Level**
1	Develop and understand the simple VHDL programs for different circuits	CO7	L3
2	Represent the flip flops as state diagram, characteristic equation	CO8	L3
b	***Course Schedule***		
Class No	**Portion covered per hour**	**-**	**-**
1	Introduction to VHDL: VHDL description of combinational circuits	CO7	L2
2	VHDL Models for multiplexers	CO7	L3
3	VHDL Modules.	CO7	L3
4	Latches and Flip-Flops: Set Reset Latch, Gated Latches	CO8	L3
5	Edge-Triggered D Flip Flop 3	CO8	L3
6	SR Flip Flop, J K Flip Flop	CO8	L3
7	T Flip Flop, Asynchronous Sequential Circuits	CO8	L3
8	Flip Flop with additional inputs	CO8	L3
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	VHDL hardware description language and its application to digital hardware design and verification.		
2	Flip flops can be used to store the data and frequency divider		
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	Explain the VHDL models.	CO7	L2
2	Write a note on VHDL Models for multiplexers	CO7	L2
3	Describe combinational and sequential circuit.	CO7	L2
4	What is latch and flip flop?	CO8	L2
5	Explain with truth table derivation for SR latch	CO8	L3
6	Explain RS and Gated Flip Flops.	CO8	L3
7	Explain edge triggered D and JK Flip Flops	CO8	L3
8	Derive the characteristic equation for SR, D , T and JK fli flop.	CO8	L3
9	Explain the +ve edge triggered SR, D , T and JK fli flop with timing diagram	CO8	L3
10	Explain the -ve edge triggered SR, D , T and JK fli flop with timing diagram	CO8	L3
e	**Experiences**		
1			
2			
3			

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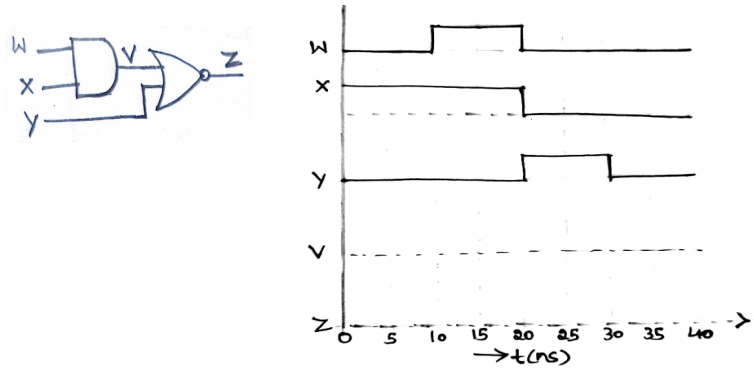
E2. CIA EXAM – 2

a. Model Question Paper - 2

Crs Code:		18CS33	Sem:	III	Marks:	50	Time:	90 minutes		
Course		Analog and Digital electronics								
-	**-**	**Note: Answer all questions, each carry equal marks. Module : 3, 4**						**Marks**	**CO**	**Level**
1	a	Complete the timing diagram for the given circuit along with the truth table. Assume that both gates have a propagation delay of 5ns. 							CO5	L4	5
	b	Implement the following function using 8:1 multiplexer f(a,b,c,d) = Σ m (0,1,5,6,8,10,12,15).							CO5	L3	6
	c	Write a Short note on Tree state buffer.							CO6	L3	7
	d	Design a 32:1 multiplexer using 16:1 mux and 2:1 multiplexer.							CO6	L3	7
		OR									
2	a	Explain Gate delays and timing diagrams.							CO5	L2	6
	b	What is multiplexer? Design a 8:1 multiplexer using 2:1 multiplexers.							CO5	L3	8
	c	Show how using a 3:8 decoder and multi input OR gates following Boolean expressions can be realized simultaneously. a. f(a,b,c) = Σ m(0,4,6) b. f(a,b,c) = Σ m(1,2,3,7) c. f(a,b,c) = Σ m(0,5)							CO6	L3	6
	d	Write a Short note on ROM.							CO6	L2	5
3	a	Deference between Combination and Sequential circuit, Latches and Flip Flops.							CO7	L2	5
	b	With a neat logic diagram and truth table explain the working of SR Latch.							CO7	L3	10
	c	With a neat diagram and waveform explain the working of relaxation oscillator.							CO8	L2	10
		OR									
4	a	Give characteristic table, characteristic equation and excitation table for SR, D and JK flip flop.							CO8	L3	10
	b	With a neat logic diagram and truth table explain the working of J K flip flop.							CO7	L3	7
	c	With a neat diagram explain SAR and also the code conversion tree of SAR for 1000.							CO7	L2	8

b. Assignment – 2

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions									
Crs Code:	18CS33	Sem:	III	Marks:	10	Time:	90 – 120 minutes		
Course:	Analog and Digital electronics				Module : 3,4				
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.									
SNo	**USN**	**Assignment Description**					**Marks**	**CO**	**Level**
1		Explain the gate delays and timing diagrams?					10	CO5	L2
2		Explain simulation and testing with examples.					10	CO5	L2
3		Why is a Multiplexer called a Universal logic					10	CO6	L3
4		Configure 16 to 1 MUX using 4 to 1 MUX					10	CO6	L3

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5		Implement the f(x,y,z)= ∑m(0,4,5,6) function using 8to1 MUX	10	CO6	L3
6		Define parity generator and parity checker	10	CO6	L3
7		Design 3 - 8 decoder	10	CO6	L3
8		Design a 32 to 1 multiplexer using two 16 to 1 multiplexers and one 2 to 1 multiplexer.	10	CO6	L3
9		Give seven segment decoder using PLA.	10	CO6	L3
10		Explain PLA and PAL.	10	CO6	L2
11		Explain the VHDL models.	10	CO7	L2
12		Write a note on VHDL Models for multiplexers	10	CO7	L2
13		Describe combinational and sequential circuit.	10	CO7	L2
14		What is latch and flip flop?	10	CO8	L2
15		Explain with truth table derivation for SR latch	10	CO8	L3
16		Explain RS and Gated Flip Flops.	10	CO8	L3
17		Explain edge triggered D and JK Flip Flops	10	CO8	L3
18		Derive the characteristic equation for SR, D , T and JK fli flop.	10	CO8	L3
19		Explain the +ve edge triggered SR, D , T and JK fli flop with timing diagram	10	CO8	L3
20		Explain the -ve edge triggered SR, D , T and JK fli flop with timing diagram	10	CO8	L3

D3. TEACHING PLAN - 3

Module – 5

Title:	Register and Counters	Appr Time:	08Hrs
a	***Course Outcomes***	**CO**	**Blooms**
-	At the end of the topic the student should be able to	-	**Level**
1	Illustrate the register and counter properties through truth table and timing diagram	CO9	L3
2	Interpret data conversion techniques through counter using state tables and graphs.	CO10	L3
b	***Course Schedule***	-	-
Class No	**Portion covered per hour**	**-**	**-**
1	Introduction Registers and Counters	CO9	L2
2	Registers and Register Transfers	CO9	L2
3	Registers and Register Transfers continued	CO9	L2
4	Parallel Adder with accumulator	CO10	L3
5	shift registers, Design of Binary counters	CO10	L3
6	Counters for other sequences	CO10	L3
7	Counter design using SR and J K Flip Flops	CO10	L3
8	Sequential parity checker, State tables and graphs	CO10	L3
c	**Application Areas**	**-**	**-**
-	Students should be able employ / apply the Module learnings to . . .	-	-
1	Registers are used to store the instructions	CO9	L3
2	Counters are used for counting electronic pulses and also used to convert signals	CO10	L3
d	**Review Questions**	-	-
-	The attainment of the module learning assessed through following questions	-	-
1	Mention the difference between combinational & sequential circuits with block diagram.	CO9	L2
2	Explain the operation of Jk master slave flip flop flip-flop. With logic diagram,characteristic table	CO9	L3
3	Explain the working of switch contact bounce circuit	CO9	L3
4	Derive the characteristic equation of RS JK and D flip flop	CO9	L2

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5	Draw the state diagram of RS JK and D flip flop	CO10	L3
6	List the different types of registers	CO10	L3
7	Explain the serial in serial out shift register . Show how the data is entered for data 1010	CO10	L2
8	Briefly explain the applications of registers	CO10	L3
9	Explain the ring counters and Johnson countesr	CO10	L3
10	Differentiate synchronous and asynchronous counters	CO10	L2
11	Explain the asynchronous mod 8 countes	CO10	L3
e	**Experiences**	-	-
1			
2			

E3. CIA EXAM – 3

a. Model Question Paper - 3

Crs Code:	18CS33	Sem:	III	Marks:	50	Time:	90 minutes
Course:	Analog and Digital electronics						

-	-	**Note: Answer all questions, each carry equal marks. Module : 5**	**Marks**	**CO**	**Level**
1	a	With a neat logic diagrams explain Parallel Adder with accumulator.	7	CO9	L3
	b	Design of Binary counters and explain.	8	CO10	L2
		OR			
2	a	Explain 4 bit serial in parallel out register.	6	CO9	L3
	b	Explain a 3 bit binary Ripple up counter. Give the block diagram, truth table and output	7	CO10	L2
	c	Differentiate between synchronous counter and asynchronous counters	2	CO9	L3
3	a	Design synchronous MOD — 6 counter with truth table and state diagram.	7	CO10	L3
	b	Design the digital clock	8	CO9	L3
		OR			
4	a	Explain 5 bit Resistor divider with diagram.	5	CO9	L3
	b	Explain the terms Accuracy and Resolution for D/A converter	4	C10	L2

b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	18CS33	Sem:	III	Marks:	10	Time:	90 – 120 minutes
Course:	Analog and Digital electronics				Module : 5		
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	**USN**	**Assignment Description**	**Marks**	**CO**	**Level**
1		Mention the difference between combinational & sequential circuits with block diagram.	10	CO9	L2
2		Explain the operation of Jk master slave flip flop flip-flop. With logic diagram,characteristic table	10	CO9	L3
3		Explain the working of switch contact bounce circuit	10	CO9	L3
4		Derive the characteristic equation of RS JK and D flip flop	10	CO9	L2
5		Draw the state diagram of RS JK and D flip flop	10	CO10	L3
6		List the different types of registers	10	CO10	L3
7		Explain the serial in serial out shift register . Show how the data is entered for data 1010	10	CO10	L2
8		Briefly explain the applications of registers	10	CO10	L3
9		Explain the ring counters and Johnson countesr	10	CO10	L3
10		Differentiate synchronous and asynchronous counters	10	CO10	L2
11		Explain the asynchronous mod 8 countes	10	CO10	L3

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12		Mention the difference between combinational & sequential circuits with block diagram.	10	CO9	L2
13		Explain the operation of Jk master slave flip flop flip-flop. With logic diagram,characteristic table	10	CO9	L3
14		Explain the working of switch contact bounce circuit	10	CO9	L3
15		Derive the characteristic equation of RS JK and D flip flop	10	CO9	L2
16		Draw the state diagram of RS JK and D flip flop	10	CO10	L3
17		List the different types of registers	10	CO10	L3
18		Explain the serial in serial out shift register . Show how the data is entered for data 1010	10	CO10	L2
19		Briefly explain the applications of registers	10	CO10	L3
20		Explain the ring counters and Johnson countesr	10	CO10	L3
21		Differentiate synchronous and asynchronous counters	10	CO10	L2
22		Explain the asynchronous mod 8 countes	10	CO10	L3

F. EXAM PREPARATION

1. University Model Question Paper

Course	Analog and Digital electronics					Month / Year	May /2018	
Crs Code:	18CS33	Sem:	III	Marks:	80	Time:	180 minutes	
Module	**Note**	Answer all FIVE full questions. All questions carry equal marks.				**Marks**	**CO**	**Level**
1	a	Explain the construction & working and principle of operation of an Photo diode				16 / 20	CO1	L2
	b	What are the differences between photo coupler and LED					CO1	L3
	c	Explain the Collector to base bias circuit?					CO2	L2
	d	Explain with neat sketches the operation and characteristics of Fixed base bias					CO2	L3
	e	Explain the working of Peak Detector					CO2	L2
2	a	What are Universal gates? Implement the basic gates using Universal gates only.				16 / 20	CO3	L2
	b	Using K-map find the reduced SOP form of $f(A,B,C,D)=\sum M(5,6,7,12,13)+\sum d(4,9,14,15)$.					CO3	L4
	c	Explain Duality Theorem?					CO4	L2
	d	Write the verilog code for given expression. Y=AB+CD					CO4	L4
	e	Simplify the following using Mc-Cluskey method $f=\sum M(4,8,10,11,12,15)+d(9,14)$					CO4	L4
3	a	Implement the following function using a 8:1 multiplexer: $f(a,b,c,)=\sum M(0,1,3,4)$.				16 / 20	CO5	L2
	b	What is a magnitude comparator? Explain with a neat block diagram an n-bit magnitude comparator					CO5	L2
	c	Design 7 segment decoder using PLA					CO6	L2
	d	Realize the following function using the 3:8 decoder $F_1(A, B, C)=\sum M(1,2,3,4)$, $F_2(A, B, C)=\sum M(3,5,7)$.					CO6	L4
	e	Give transition diagram of JK and T Flip flops					CO6	L3
	f	Differentiate between combinational circuit and sequential circuit					CO5	L3
4	a	Draw the logic diagram of a 4-bit serial in serial out shift register using J-K flip flop and explain.				16 / 20	CO7	L3
	b	Design a modulo-5 up counter (synchronous) using J-K flip flop					CO8	L3
	c	Difference between Asynchronous and Synchronous Counter					CO7	L3
	d	Draw the logic circuits and the excitation tables for the T, JK flip-flops.					CO8	L3
5	a	Explain with logic diagram 3 bit simultaneous A/D converters.				16	CO10	L3
	b	What is Binary ladder? Explain the binary ladder with digital input of 1000					CO10	L3
	c	Give performance parameters of DAC or D/A converters					CO10	L3
	d	Explain Digital clock with block Diagram.						L3

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2. SEE Important Questions

Course:		Analog and Digital Electronics						Month / Year	/2018	
Crs Code:		18CS33	Sem:	3	Marks:	100		Time:	180 minutes	
-	**Note**	Answer all FIVE full questions. All questions carry equal marks.						**Marks**	**CO**	**Level**
1	a	Explain the construction & working and principle of operation of an Photo diode						10	CO1	L2
	b	What are the differences between photo coupler and LED						04	CO1	L2
	c	Explain the Collector to base bias circuit?						06	CO2	L2
		OR								
-	a	Explain with neat sketches the operation and characteristics of Fixed base bias						10	CO1	L2
	b	Explain the working of Peak Detector						10	CO1	L2
2	a	What are Universal gates? Implement the basic gates using Universal gates only.						10	CO3	L2
	b	Using K-map find the reduced SOP form of $f(A,B,C,D)=\sum M(5,6,7,12,13)+\sum d(4,9,14,15)$.						10	CO4	L4
		OR								
-	a	Explain Duality Theorem?						04	CO3	L2
	b	Write the verilog code for given expression. Y=AB+CD						04	CO4	L4
	c	Simplify the following using Mc-Cluskey method $f=\sum M(4,8,10,11,12,15)+d(9,14)$						12	CO4	L4
3	a	Implement the following function using a 8:1 multiplexer: $f(a,b,c,)=\sum M(0,1,3,4)$.						10	CO5	L4
	b	What is a magnitude comparator? Explain with a neat block diagram an n-bit magnitude comparator						05	CO5	L4
	c	Design 7 segment decoder using PLA						05	CO6	L2
		OR								
-	a	Realize the following function using the 3:8 decoder $F_1(A, B, C)=\sum M(1,2,3,4)$, $F_2(A, B, C)=\sum M(3,5,7)$.						10	CO5	L4
	b	Give transition diagram of JK and T Flip flops						06	CO6	L2
	c	Differentiate between combinational circuit and sequential circuit						04	CO6	L2
4	a	Draw the logic diagram of a 4-bit serial in serial out shift register using J-K flip flop and explain.						10	CO8	L2
	b	Design a modulo-5 up counter (synchronous) using J-K flip flop						10	CO8	L4
		OR								
-	a	Explain Johnson Counter with neat diagram and timing diagram						10	CO7	L4
	b	Difference between Asynchronous and Synchronous Counter						04	CO8	L2
	c	Draw the logic circuits and the excitation tables for the T, JK flip-flops.						06	CO7	L4
5	a	Explain with logic diagram 3 bit simultaneous A/D converters.						10	CO10	L4
	b	What is Binary ladder? Explain the binary ladder with digital input of 1000						10	CO10	L4
		OR								
	a	Give performance parameters of DAC or D/A converters						10	CO10	L4
	b	Explain Digital clock with block Diagram.						10	CO9	L4
-										

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G. Content to Course Outcomes

1. TLPA Parameters

Table 1: TLPA – Example Course

Module-#	Course Content or Syllabus (Split module content into 2 parts which have similar concepts)	Content Teaching Hours	Blooms' Learning Levels for Content	Final Blooms' Level	Identified Action Verbs for Learning	Instruction Methods for Learning	Assessment Methods to Measure Learning
A	B	C	D	E	F	G	H
1	Photodiodes, Light Emitting Diodes and Optocouplers ,BJT Biasing :Fixed bias ,Collector to base Bias , voltage divider bias.	04	L2	L3	1.Identify 2. Diodes Application	Chalk & Board	Questionnaire and Assignment
1	Operational Amplifier Application Circuits: Multivibrators using IC-555, Peak Detector, Schmitt trigger, Active Filters, Non-Linear Amplifier, Relaxation Oscillator, Current-to-Voltage and Voltage-to-Current Converter , Regulated Power Supply Parameters, adjustable voltage regulator ,D to A and A to D converter.	04	L3	L3	1. Understand 2. Opamp application circuits	Chalk & Board	CIA
2	Karnaugh maps: minimum forms of switching functions, two and three variable Karnaugh maps, four variable karnaugh maps, determination of minimum expressions using essential prime implicants	04	L4	L4	1. Understand 2. Logic gates fundamentals	Chalk & Board	CIA
2	Quine-McClusky Method: determination of prime implicants, The prime implicant chart, petricks method, simplification of incompletely specified functions, simplification using map-entered variables	04	L4	L4	1.Understand 2. Boolean equation simplification	Chalk & Board	CIA and Assignment
3	Combinational circuit design and simulation using gates: Review of Combinational circuit design, design of circuits with limited Gate Fan-in ,Gate delays and Timing diagrams, Hazards in combinational Logic, simulation and testing of logic circuits	04	L2	L3	1. Understand 2. Data processing circuits design	Chalk & Board	CIA and Assignment
3	Multiplexers, Decoders and Programmable Logic Devices: Multiplexers, three state buffers, decoders and encoders, Programmable Logic devices, Programmable Logic Arrays, Programmable Array Logic.	04	L3	L3	1.Understand 2. Combinational circuit applications	Chalk & Board	CIA & Assignment
4	Introduction to VHDL: VHDL description of combinational circuits, VHDL Models for multiplexers, VHDL Modules.	04	L2	L3	1. Comprehend 2.VHDL models	Chalk & Board	CIA and Assignment

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4	Latches and Flip-Flops: Set Reset Latch, Gated Latches, Edge-Triggered D Flip Flop 3,SR Flip Flop, J K Flip Flop, T Flip Flop, Flip Flop with additional inputs, Asynchronous Sequential Circuits	04	L3	L3	1. Understand 2. Flip flop Operation	Chalk & Board	CIA and Assignment
5	Registers and Counters: Registers and Register Transfers, Parallel Adder with accumulator, shift registers	04	L3	L3	1.Understand 2.Register Design	Chalk & Board	CIA and Assignment
5	design of Binary counters, counters for other sequences, counter design using SR and J K Flip Flops, sequential parity checker, state tables and graphs	04	L2	L3	1. Understand 2.Counters Design	Chalk & Board	CIA and Assignment

2. Concepts and Outcomes:

Table 2: Concept to Outcome – Example Course

Module-#	Learning or Outcome from study of the Content or Syllabus	Identified Concepts from Content	Final Concept	Concept Justification (What all Learning Happened from the study of Content / Syllabus. A short word for learning or outcome)	CO Components (1.Action Verb, 2.Knowledge, 3.Condition / Methodology, 4.Benchmark)	Course Outcome **Student Should be able to ...**
A	I	J	K	L	M	N
1	Know the operation of diodes in different application circuits	Diodes Application circuits	Diodes	Diodes Application circuits	1.Identify 2. Diodes Application	Understand the operation of diodes in different application circuits
1	Explaining the operation amplifier application circuits	Opamp application circuits	Opamp	Opamp application circuits	1. Understand 2. Opamp application circuits	Understand the operation amplifier application circuits
2	Apply the knowledge of fundamentals of logic gates through truth table	Logic gates fundamentals	Logic gates	Logic gates fundamentals	1. Understand 2. Logic gates fundamentals	Understand the fundamentals of logic gates through truth table
2	Simplify Boolean equations by different methods	Boolean equation simplification	Boolean equation	Boolean equation simplification	1.Understand 2. Boolean equation simplification	Simplify Boolean equations by Karnaugh map and Quine MCClusky method to design combinational circuits
3	Designing of expressions using different gates	Data processing circuits design	Data processing circuits design	Data processing circuits design	1. Understand 2. Data processing circuits design	Design data processing circuits using combination of gates
3	=combinational circuits working with	Combinational circuit	Combinational circuit	Combinational circuit applications	1.Understand 2. Combinational circuit applications	Understand the fundamentals of combinational

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	truth table and timing diagram	applications				circuits by truth table and timing diagram
4	write simple VHDL programs for different circuits	VHDL models	VHDL	VHDL models	1. Comprehend 2.VHDL models	Develop and understand the simple VHDL programs for different circuits
4	Writing flip flops state diagram, characteristic equation	Flip flop Operation	Flip flops	Flip flop Operation	1. Understand 2. Flip flop Operation	Represent the flip flops as state diagram, characteristic equation
5	Designing the Registers	Register Design	Register	Register Design	1.Understand 2.Register Design	Illustrate the register and counter properties through truth table and timing diagram
5	Designing the counters	Counter Design	Counter	Counter Design	1. Understand 2.Counters Design	Interpret data conversion techniques through counter using state tables and graphs.

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